Project Planning

Introduction

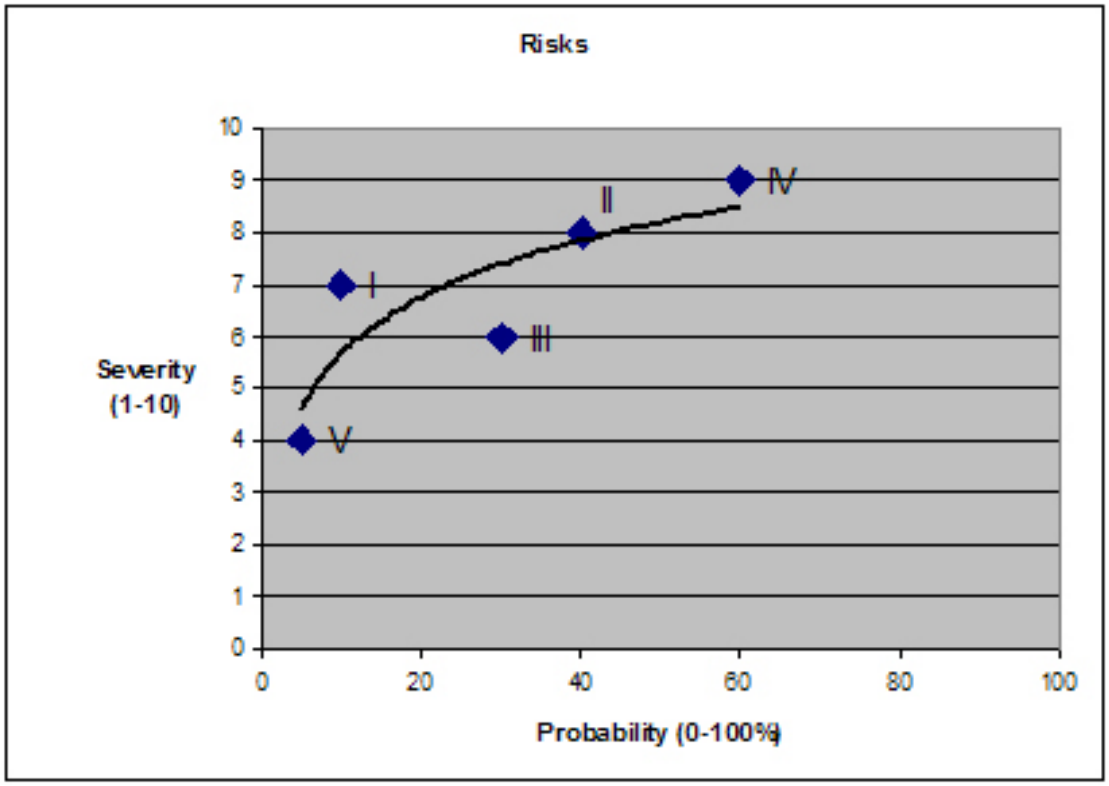
In this section, the plans required for completing the project from start to finish are described. The risk analysis section of this project plan will describe the potential items of risk for the intended design. The rated severity and probability of each risk will allow a comparison to be made amongst the risks. In particular, a threshold line on the plot of severity versus probability will permit a critique to be performed upon the risks. In the mitigation strategy, plans are described for addressing each of the risks which lie above the threshold line. The work breakdown structure offers an overview of the main areas of work in the project , largely the high level tasks. The responsibility matrix describes the higher level tasks of the project, and also lists who has responsibility for each task. The final part of the project plan is the project schedule which consists of a Gantt chart that lists the detailed tasks of the project as well as who has responsibility for them. A tracking Gantt chart is also shown which lists the completed tasks and the tasks which are in progress.

Risk Analysis

Risk	Risk Title	Severity (1-10)	Probability (0-100%)
I	FPGA Area	7	10
II	Timing	8	40
III	Input Distortion	6	30
IV	Synchronization	9	60

V	Work Force	4	5

- FPGA Area: Since the intended design is to be implemented directly onto the FPGA, the area the design takes up is crucial. It should be able to operate without conflicting with the existing technology on the board.
- Timing: A key risk to this design is that each of the components of the design operate at different frequencies. The pulses that will be detected are too fast to be recognized by the FPGA. The design must be able to account for and handle all the different frequencies it is presented with.
- Input Distortion: As a matter of testing the device, a signal generator will be used. The risk here is ensure the integrity of the input signal as it's passed to our design. Therefore, if the signal is distorted on our way to the device, it will be useless in testing the functionality of the detector.
- Time Synchronization: Related to the timing. The computer running the GUI will be running on an entirely different clock, and therefore synchronizing the signals will be a risk. The GUI must be able to properly display the collected signals without dropping information due to the asynchronous clocks.
- Work Force: Information must be learned and incorporated to build the detector. A large risk is that the material needed to be understood to build this design might not be able to be learned, or learned well enough in the time frame.



Mitigation Strategy

- Too large: The design takes up too much room on the FPGA. If this occurs the design will need to be reworked to remove unnecessary logic or in the worst case scenario the design can change to a sticky bit configuration. The sticky bit has a number of drawbacks over the logic analyzer approach but it would take up less area.
- Unable to meet timing: If the finished design turns out to be too slow and is unable to meet timing requirements the only feasible solution is to switch to the sticky bit configuration. The sticky bit would certainly be able to capture the 5ns pulse but it would be at the expensive of being able to measure a quick succession of pulses.
- Distortion of input: If the standard ribbon cables cause too much distortion on the input then the simulated sensor signal will have to use a more complex and expensive wire to carry

the signal from the signal generator to the FPGA header pins.

- Time Synchronization: There is the potential for problems to exist when translating the measured event pulses to the GUI. This could be mitigated by using a counter to produce a time code that is stored with the pulses. This time code could then be passed to the GUI ensuring that the pulses are displayed accurately.
- Learning New Material: There is a risk that learning all of the material that is associated with the project could prove to be difficult. If problems occur the mitigation is to seek expert advice from professors that would be knowledgeable about the specific problem or from students that have performed research in the area.

Work Breakdown Structure

- Event detector design and simulation. This encompasses the development of the VHDL code needed to describe the event detector on the FPGA as well as the simulation work that is needed to verify that the event detector is functioning normally.
- Com port design. The data from the FPGA is stored in a RAM and is then transferred to the computer using an RS-232 cable. The speed that the FPGA and the computer are running at are different therefore a VHDL code is going to be produced to synchronize those two pieces of hardware together.
- GUI design. A graphical user interface will be designed to read the data collected by the design. It will read the data via the RS-232 cable and displayed. All 32-channels of the device will be displayed to show the location of a strike.

Responsibility Matrix

Trevor Hendricks: Event detector vhdl design and simulation

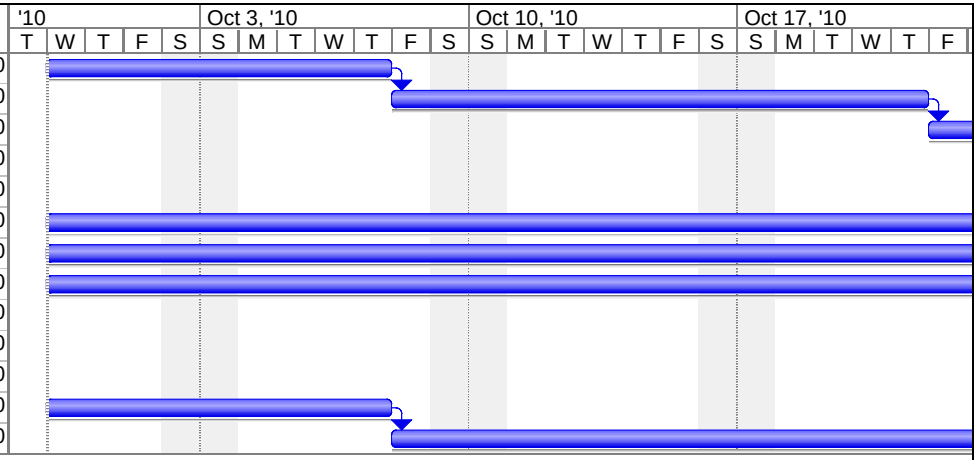
Midhat Feidi: Com port VHDL design

Andrew Szatkowski: GUI

Project Schedule

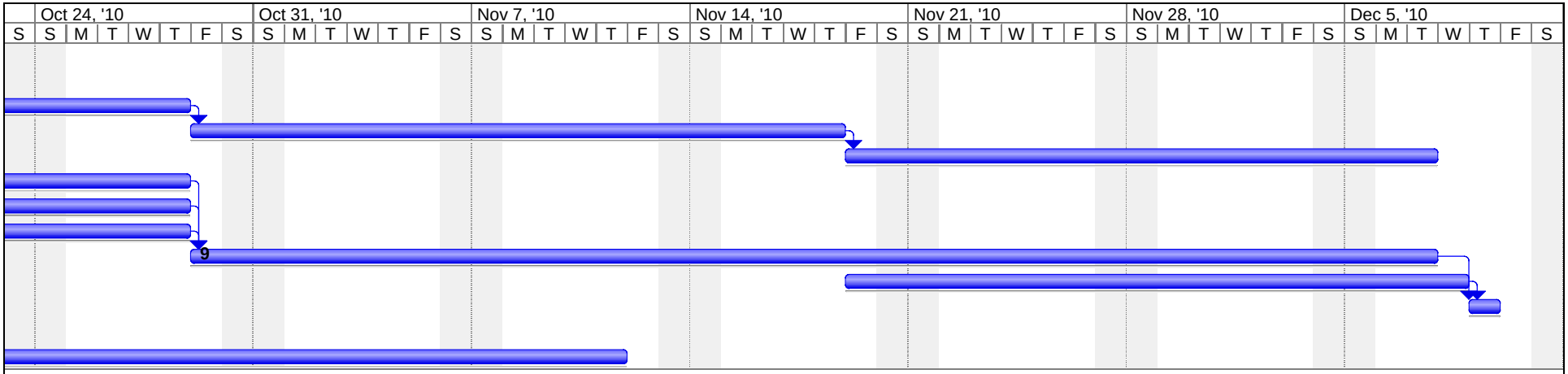
see attached Gantt chart.

ID	Task Name	Duration	Start	Finish
1	Concept Development	7 days	Wed 9/29/10	Thu 10/7/10
2	System Architecture	10 days?	Fri 10/8/10	Thu 10/21/10
3	Detailed Design	5 days?	Fri 10/22/10	Thu 10/28/10
4	Analysis and test	15 days?	Fri 10/29/10	Thu 11/18/10
5	Assemble Report	13 days?	Fri 11/19/10	Tue 12/7/10
6	COM system VHDL	22 days?	Wed 9/29/10	Thu 10/28/10
7	Event Detector VHDL and Simulations	22 days?	Wed 9/29/10	Thu 10/28/10
8	GUI design	22 days?	Wed 9/29/10	Thu 10/28/10
9	System Integration	28 days	Fri 10/29/10	Tue 12/7/10
10	Design Poster Creation	14 days	Fri 11/19/10	Wed 12/8/10
11	Design Fair and Project Demo	1 day	Thu 12/9/10	Thu 12/9/10
12	Draft of web page	7 days?	Wed 9/29/10	Thu 10/7/10
13	Finished Webpage	25 days	Fri 10/8/10	Thu 11/11/10



Project: gantt_chart
Date: Wed 9/29/10

Task
Split
Progress
Milestone
Summary
Project Summary
External Tasks
External Milestone
Deadline



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Task		Milestone		External Tasks	
Split		Summary		External Milestone	
Progress		Project Summary		Deadline	