Concept Development

Introduction

In this section, a full understanding of the selected design will be laid out. The concept design will describe the design which was selected via the decision matrix. More particularly, the details of the design will be described in depth in order to further clarify the functionality of the product. The evaluation criteria utilizes outside opinions, particularly that of the public, as a means of refining the design parameters. Interviews are used to gain new opinions about whether particular functions are necessary in the design. More importantly, the results of the interviews can alter the design by affirming a decision upon whether or not specific functions should be kept. From the feedback of the evaluation criteria, the functions of the design can be revisited in order to develop a convergence plan. A convergence plan consists of the merger of functions between the new, a result of the interviews, and the old. The ideas then converge into a new design intention known as the convergence plan. The final aspect of concept development is the contingency plan which accounts for the possibility that a given design might fail further along in the design process. By having a set of prescribed contingencies, a backup plan is formed as a means of mitigating a complete design overhaul.

Concept Design

From the decision matrix that was created earlier in this project, it was concluded that a logic analyzer design ???? . The general idea is that a group of simple D flip flops will be able to be clocked at high speed to be able to record the high speed transient inputs from the radiation

sensor that must be recorded. These flip flops can then serve as a demux. This will turn a single high speed channel into multiple low speed inputs. The current tentative design will clock the flip flops at 400 MHz and turn the signal into a four channel 100MHz output. This output will then be stored into a dual clock RAM which will allow the values to be stored in and then pulled out at different clock. This serves to synchronize the output with the clock of the majority of the FPGA. There will be a counter that will be clocked at 100MHz and this counter will then be used to provide the address for writing to the RAM.

The part described above will serve as the main event detector logic. This will then be followed by some logic that will read from the memory and format it to be passed to the UART block of logic. The UART logic block will properly format the data into bytes to be sent over RS232 to the GUI. The GUI will receive the data over RS232 and plot the data from each of the channels. This will show where and when radiation strikes were detected on each of the 32 channels of the sensor.
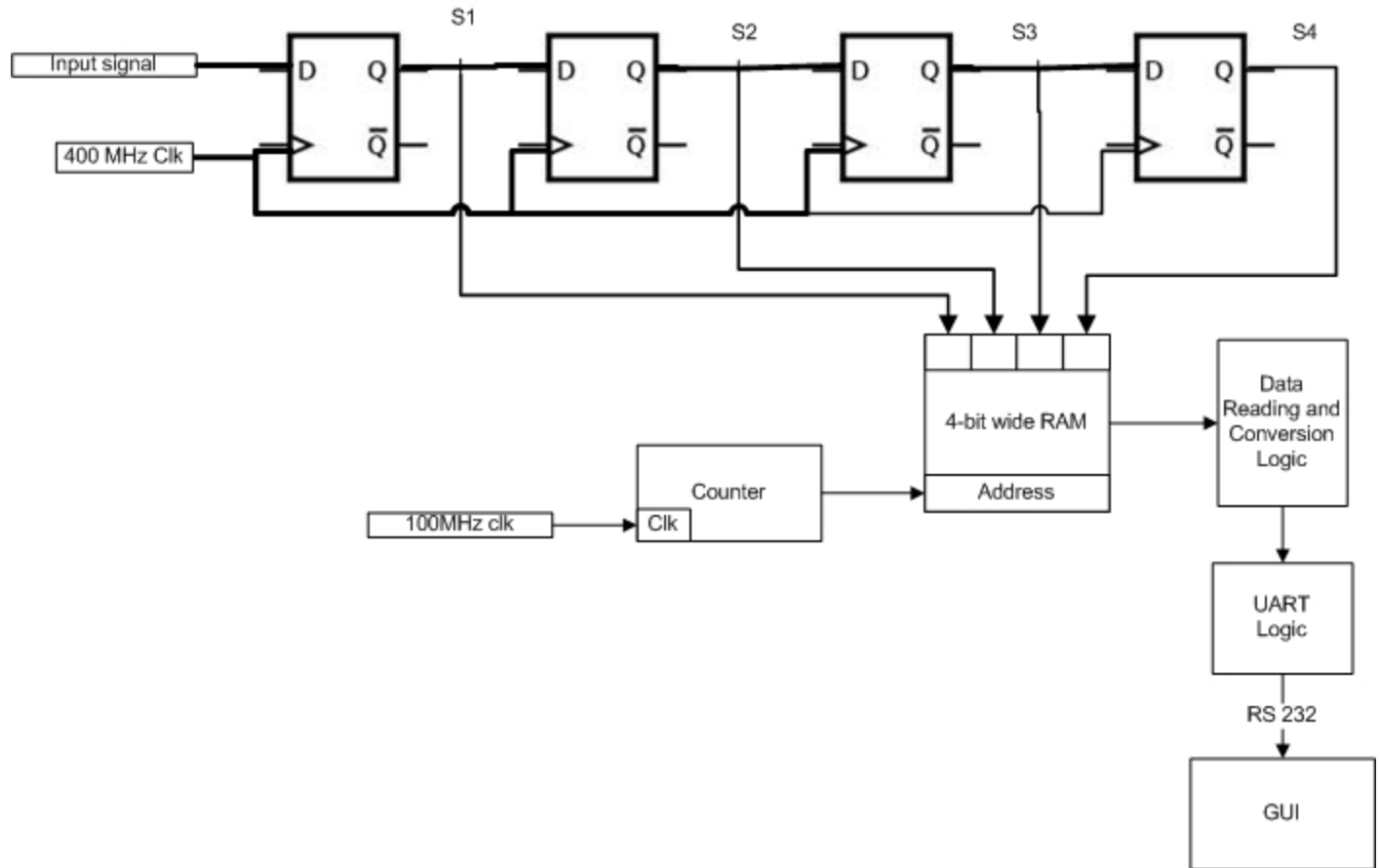
Figure 1: A system level flowchart showing the system.

NOTE: Figure 1 shows all of the logic for 1 of the 32 sensor channels

      The FPGA will communicate with the PC running the GUI using RS232. The RS232

sends one byte packets. The FPGA will only send packets for the positive hits and it will not

send packets for no strikes. This means that the packet must also enclose time information along

with the channel information. There are 32 sensor channels so that means that there are four bits

for channel information. The RAM is 4 bits wide and each bit could contain a radiation event so

it is important to know which bit the strike took place in. This means there will be 2 bits devoted

to location information. That leaves 2 bits to be used for the memory address. This limits the memory of each channel to four four bit memory locations. The final byte that gets transferred over RS232 to the GUI will have two leading bits as the address, then two bits for the location, and then the four least significant bits will be used to identify the channel of origin.

Evaluation Criteria

Interview with Andrew Shull - Electrical and Computer Engineering

Andrew has had experience in working with FPGAs and various digital systems. When talking with Andrew his main concern with our design was the need for us to define communication protocols for our design early on. He felt that waiting to clearly define the way that the different portions of the design communicated with each other could lead to significant problems down the line once a standard is decided upon. His opinion was that the sooner the standard is decided the less work will have to be redone in order to integrate all of the portions of the design together. Andrew also felt that in that spirit we must consider how we will transmit the data and deal with the limited bandwidth of the UART RS232 protocol. He also felt it is worth considering whether we need to implement a system to verify data transmission integrity.

Interview Summary

After performing interviews a main theme is that it is important to perform the development early and at the very start of the development decide on all the standards for communicating between sections of the design. This will help alleviate some of the stresses that are sure to occur as the design deadlines approach. The interviews did not bring to light any

major design modifications though because the design has had all of the desired specifications from NASA from the beginning of the design process. This has mitigated the need for any significant redesigns.

Convergence Plan

After further analyzing our event detector design there have been several decisions that were made. One of the decisions was to quickly settle on a communications protocol. This protocol is described above in the concept design portion of this report. It is also important to create the VHDL so that it is very simple and can run at the high speeds required for the desired performance. At this point there are limited design modifications required because the specifications were well defined from the beginning of the project.

Contingency Plan

Our contingency plan is the sticky-bit design. It scored almost nearly as high as the logic analyzer in the decision matrix. The number one drawback to this approach is that it makes one drastic assumption. If it is safe to assume that there will not be 2 consecutive strikes on the same channel, this idea would be preferred. The advantage of this approach would be a slightly smaller footprint on the FPGA along with a slightly simpler logic design. This simpler logic could possibly allow for a faster clock with this design. If the design progresses and timing becomes a significant issue the sticky bit design could be used instead of the logic analyzer design.

If the sticky bit is employed there is the significant drawback of losing the ability to detect multiple strikes. This has a second effect of providing significantly lower resolution for the demo. Instead of being able to show the sensor signals at 2.5ns intervals the sticky bit will

only show 10ns intervals. However, the sticky bit design would allow for a longer viewing

period with the same memory usage.